CMOS image sensor architecture for high-speed sparse image content readout

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Abstract
Many high-end imaging systems make use of high-speed image sensors. With resolution ranging from 1 to 4 Mpixels and with readout speed of several thousands of frames per second, these image sensors are very large circuits. They consume usually several Watts and are complex to use and interface due to the large amount of high bandwidth parallel analog busses. However, in various cases where high-speed image sensors are required, it appears that the scene contains sparse, yet fugitive, information.

To address this issue, we propose first a novel architecture, for image sensor readout using a pipelined global shutter image sensor in which the readout is asynchronous and not scanned sequentially. Content aware pixels use a domino-like asynchronous readout and do not suffer from ambiguity during the decoding of the addresses. The analog data are then retrieved from the single pixels using the asynchronously read addresses. We present the concept and design. We discuss the required payload in term of pixel surface to perform such operation.

1 Principle

1.1 Introduction

In many scientific applications where imaging is involved, events of interest are rare and fugitive. For research subjects like Particle Detection [1] or High Atmosphere Lightning Study [2], high-speed imagers are required to operate with readout times with an order of magnitude between 100us and 1ms. However, fully synchronous high-speed image sensor are extremely inefficient in terms of power. Moreover it is difficult to reach a high resolution with such sensors, as the amount of data is dramatically high. Following the developments of retina-like image sensors [3], a solution to this bottleneck issue has been to realize most of the image processing in the pixel to minimize the amount of data to be read [4, 6-11]. For instance, images that are post-processed afterwards in a region of interests may benefit from such image pre-processing. The example of Achard's algorithm is well-known in this respect. In many image interpreting applications, apart from the extracted information, the analog pixel intensities themselves are desired too. The idea is thus to use the same principle as in retina-like approach, and to still be able to retrieve the analog data.

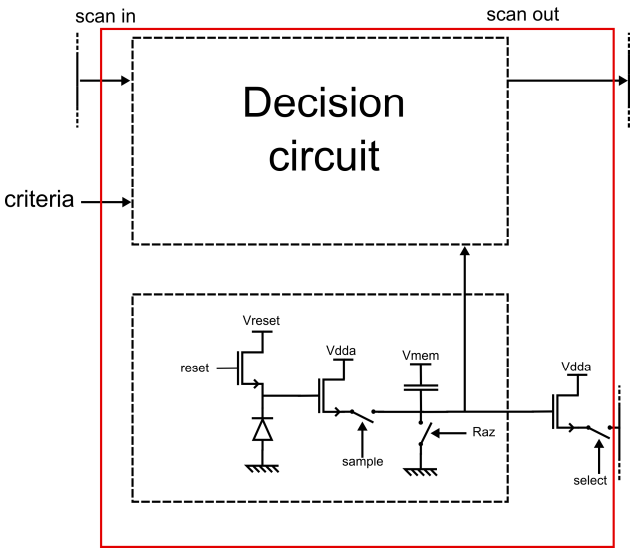

Figure 1 generic pixel floor plan

1.2 Proposed solution

We propose to use a snapshot capable pixel in which the data readout and the light integration are not interdependent. The actual readout phase follows an identification phase meant to sort pixels prior to readout. Several options are discussed in this paper to sort those pixels. Sorting can be realized asynchronously, meaning that the duration of the sorting phase depend on the actual number of pixels of interests, or synchronously scanned using a novel fast-scan method described later in this paper.

A common topology for such pixels can be defined as presented in **Fout! Verwijzingsbron niet gevonden.**. The analog front-end is a synchronous pipelined snapshot shutter pixel. The difference between fully asynchronous sensors [5] and our method resides in the fact that an event can be logged in time with the proposed method with the frame (integration) time granularity. As all analog data are sampled simultaneously, there is no ambiguity. The pixel further contains a generic decision circuit with binary output. It can be as simple as a comparator (E.g. when the pixel voltage is above a given voltage criterion) or execute a complex

algorithm. A positive output means that the pixel contains data that are interesting to be read. The decision circuit contains also elementary propagation logic to execute a sparse scan.

2 Hardware implementations

2.1 Digital implementation

The first proposed implementation is a domino-like test propagation in the decision circuit as shown in Figure 2. Here the propagation of the test is performed by a fully digital circuit. The corresponding equations are:

$$\left.\begin{aligned} M &= I_H \bullet D + (I_H + \overline{I_V}) \bullet M \\ O_V &= I_V + M \bullet \overline{I_H} \\ O_H &= I_H + I_V + M \end{aligned}\right\} \quad (1)$$

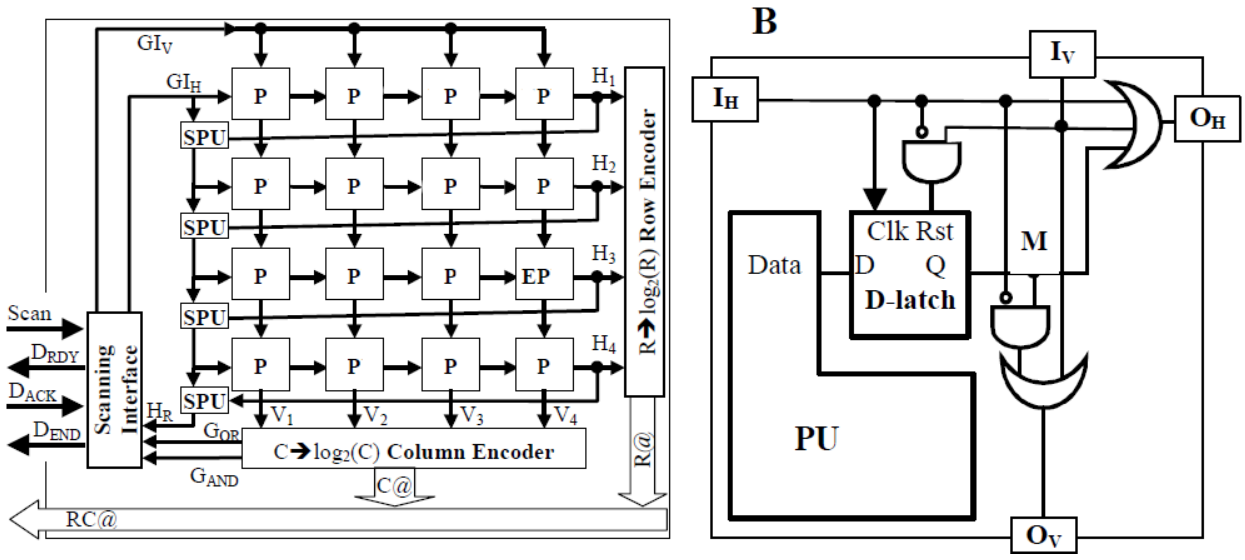

Figure 2: asynchronous test propagation floor plan

The principle is the following. The integration time start after resetting the photodiode. The integration time ends when the pixel data are sampled on the sample capacitors of **Fout! Verwijzingsbron niet gevonden.**. Then a scan is initiated by introducing a rolling '1' in the scan chain that propagates following a zig-zag pattern until it reaches a "pixel of interest". This pixel issues then a column and line signal that triggers an interruption to the user by asserting D_{RDY} The user can then read the pixel and acknowledge the interruption using D_{ACK}.

The global reading time of the array depends on N_{ACT}, the number of pixels of interest cells. The speed of scanning architecture is characterized by the horizontal / vertical falling to falling edges delays t_{H00}, t_{V00}, rising to rising edge delays t_{H11} and t_{V11}, and the row / column encoding delays t_{ENC_R} and t_{ENC_C}. The row and the column encoding processes are concurrent. Let's assume t_{ENC} as the worst of two delays. The external controller speed plays a role as well. It is characterized by its reading delay t_{R_EX}. So the global reading time is:

$$t_{SCAN} = R\,C\,(t_{H00} + t_{H11}) + N_{ACT}\,R\,(t_{V00} + t_{V11}) + N_{ACT}\,(t_{ENC} + t_{READ})$$

In this situation readout and scanning are interleaved. The performance estimation in terms of power budget has been simulated using Matlab and compared to an actual 512x512 CMOS image sensor. Results are presented on Figure 3. The disadvantage of this structure is the large amount of digital electronic requires just to realize the a scanning process. The actual digital payload to do so is 15 Transistors per pixel, which are in most cases not acceptable from optical performance and density point of view.

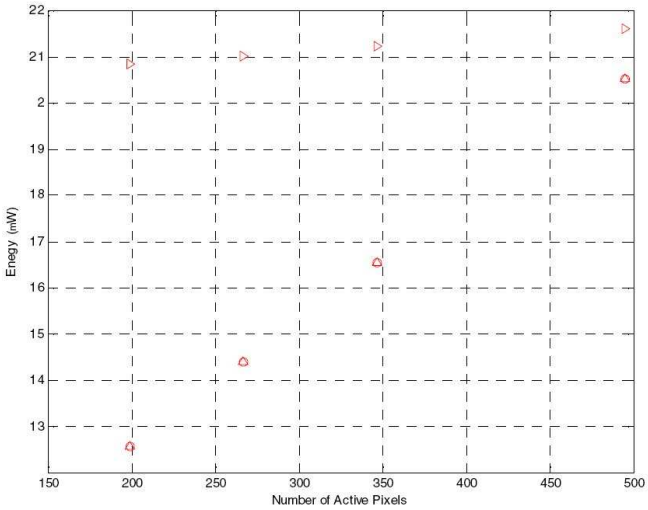

Figure 3: Energy consumption for rolling shutter APS (horizontal triangles) and Asynchronous Scans (circles) as a function of the quantity of effective information in the image for a 512x512 imager @30 fps.

2.2 Fast scan implementation

To overcome the limitation of the previous readout scheme, we propose a less intrusive pixel design. The in-pixel decision maker electronic remains unchanged but the digital scanning mechanism is greatly simplified: the scan electronic is limited to only two extra transistors. This approach consists of using a fast scan operation to locate pixels of interests scanning the array one column after the other. The image sensor floor plan is presented in Figure 4. A shift register propagates a logical '1' along the columns. When at least one pixel of the selected column is active, its corresponding switch is closed and a logical '1' is set on its row. A column asynchronous scan on the side of the pixel array allows to scan the active rows one by one. A row encoder yields the corresponding address of the pixel. Once all the addresses of have rows of the selected column have been read, the shift registers shifts the logical '1' to the next "active" column.

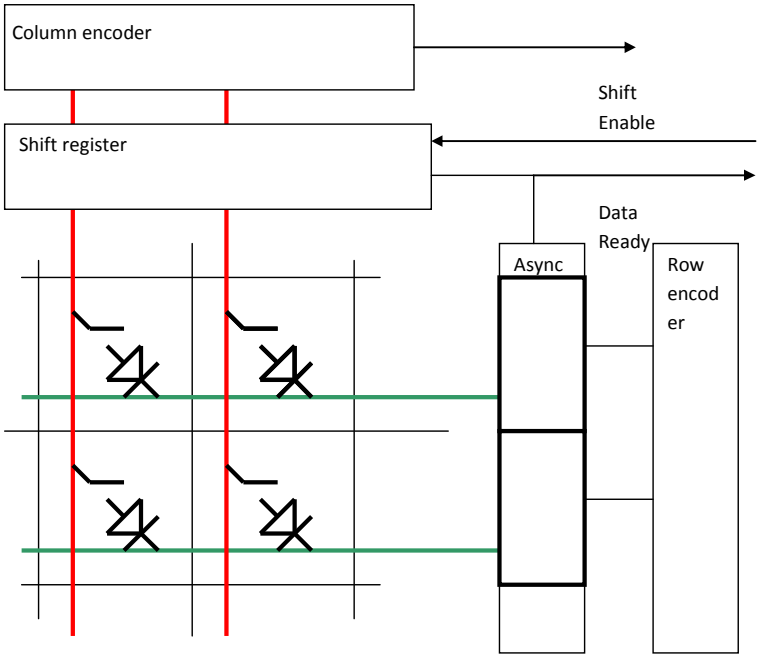

Figure 4: fast scan conceptual pixel array.

The pixel floor plan is presented on **Fout! Verwijzingsbron niet gevonden.**. As in the previous case, all pixels are reset, exposed and sampled simultaneously. Compared to the scheme of Figure 4, the diode functionality is implemented by 2 transistors. A row is accessed by asserting X_{scan}. If a pixel is of interest ("active"), the vertical Y_{output} colomn signal becomes a logical '1'. This requires that the Y_{output} columns are precharged to a logical '0'. Several X-positions can be "active" per line. Even if all pixels in a row are "active", this process is much more efficient than the classic analog readout where the row overhead time can be significant. E.g. using a .35µm CMOS technology on a 512x512 array, the row overhead time is estimated 3.5µs for analog readout , while it is less than 0.1 µs for binary readout. For the same

reason, the output of the digital pixel position to the output is much faster than classic readout analog pixel data. Considering the worst case of having 512 active pixels spread over the 512 columns, the read out time is given by:

$$Tscan = N_{Col}\left(t_{pCol} + N_{Row} \times t_{pAs} + t_{encod} + t_{read}\right)$$

Where N_{col} is the number of columns, N_{Row}, the number of rows, t_{pcol} the rise time along a column, t_{pAs}, the propagation time for one cell of the asynchronous scan, $t_{encod} + t_{read}$ gives the time required to retrieve the address of the active row and to enable the shift register to shift. The worst case scan time (all pixels activated) is a few 100µs for the whole array. Afterwards, analog readout may take place where the pixels of interest have been identified.
The energy required to perform the reading is mainly due to the propagation of the logical '1' around the column and to the propagation of information within the asynchronous scan. The shift register requires 10nJ/column with our chip while the asynchronous reading of active rows is about 30nJ/row.

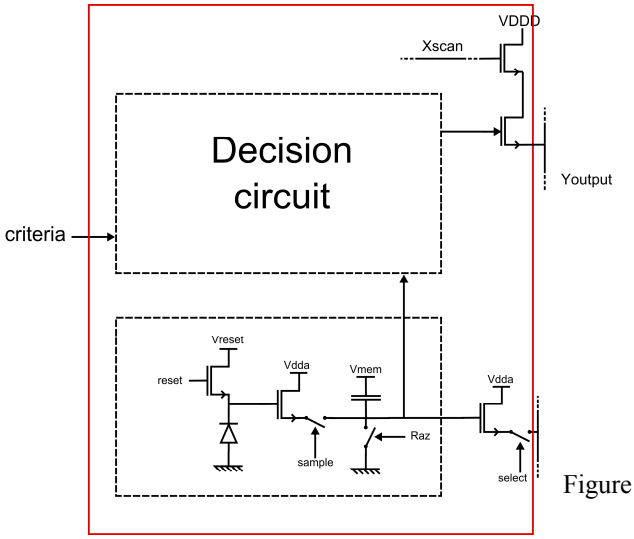

Figure 5 Fast scan pixel

3 Conclusions and Perspectives

The asynchronous scan enables a very fast and power saving reading of sparse information binarized preprocessed images. We have condensed the original concept to asynchronous scan method that requires only 2 extra transistors per pixel. With this implementation, even if few lines or columns can be skipped, the reading of pertinent information is still accelerated since the most time and energy-consuming steps (i.e. decoding the pixel positions) are fast compared to analog readout.

4 References

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